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EXAMINER	
ALROBAYE, IDRISS N	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/593,695	NAKASHIMA, YASUHIKO	
	Examiner	Art Unit	
	IDRISS N. ALROBAYE	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17,30 and 31* is/are pending in the application.

4a) Of the above claim(s) *18-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,30 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/20/2006 & 2/12/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to applicant's election/restriction received on 01/23/2009.

2. Claims 1-17, 30 and 31 presented for examination. Claims 18-29 withdrawn.

Election/Restrictions

3. Applicant's election of claims 1-17 and 30-31 in the reply filed on 01/23/2009 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 30 "*a data processing program, causing a computer to execute processes carried out by the means of the data processing device",* and claim 31 "*A computer-readable storage medium".*

6. A substitute specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b) is required. The substitute specification filed must be accompanied by a statement that it contains no new matter. Furthermore, see rejections under 35 USC 112 1st and 2nd paragraph where the current claim language is not clearly explained in the specification. Therefore, the substitute specification must provide a clear explanation of claim limitations.

Claim Objections

7. Claims 16-17 are objected to under 37 CFR 1.75(c) as being in improper form because they reference back to another multiple dependent claim 15.

Claim 30 is objected because it depends on claims 18-29 which are withdrawn.

Claim 31 is objected to as being in improper form because it reference back to another multiple dependent claim 30.

Information Disclosure Statement

8. The information disclosure statement filed 9/20/2006 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

For instance, the two NPL documents "A Speedup Technique with Function level Value Reuse and Parallel Precomputation" and "Information Processing Society of Japan“ Journal: High Performance Computing System" were provided in Japanese but no English translation. The two NPL documents have been placed in the application file, but the documents have not been considered.

Furthermore, KR 10-2005-0108343A has been placed in the application file but has not been considered because there is not translation, not even translation for the abstract.

Claim Rejections - 35 USC § 101

9. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10. Claim 30 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

11. As per claims 30, the claims would have reasonably interpreted as software alone and thus lack the necessary physical articles or objects to constitute a machine or a manufacture within the meaning of 101. It is clearly not a series of steps or acts to be a process nor is it a combination of chemical compounds to be a composition of matter. As such, it fails to fall within a statutory category. It is, at best, functional descriptive material per se.

Claim Rejections - 35 USC § 112

12. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

13. Claims 1-17, 30-31 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

14. As per claim 1, the claim recites "*input/output generating means for generating an input/output group which is made up of an input pattern and an output pattern at the time of execution of the instruction region by the first computing means",* the i/o group which is made up of input/output pattern was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification merely recites same limitation but did not describe it in the specification in such a way as to enable one skilled in the art to which it pertains.

Furthermore, the specification merely recites "matching pattern", "performing reuse", "input/output element" and "pattern derives" but the specification did not describe in such a way as to enable one skilled in the relevant art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

15. As per claims 2-3, taking claim 2 as exemplary, the claim recites "in a case where a first group of input elements from which a first output element derives is all included in a second group of input elements from which a second output element different from the first output element derives, the input/output group setting means", The specification merely recites same limitation but did not describe in the specification in such a way as to enable one skilled in the art to which it pertains.

16. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

17. Claims 1-17, 30-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

18. As per claim 1, the claim recites "*input/output generating means for generating an input/output group which is made up of an input pattern and an output pattern at the time of execution of the instruction region by the first computing means",* the i/o group which is made up of input/output pattern is vague and indefinite. There is no explanation as to what i/o group or i/o pattern pertains to. The specification merely recites the same limitation but no further description of the limitations. The MPEP, in particular, rather than requiring that the claims are insolubly ambiguous, holds that if a claim is amenable to two or more plausible claim constructions, the USPO is justified in requiring the

applicant to more precisely define the metes and bounds of the claimed invention by holding the claim unpatenable under 35 USC 112, second paragraph, as indefinite.

19. Claim 1 further recites "*at the time of execution of the instruction region, if the input pattern of the instruction region is matched with an input pattern stored in the instruction region storage means, the first computing means performing reuse so that the output pattern, which is stored in the instruction region storage means in association with the input pattern, is outputted to the register and/or the main memory means*", this limitation is vague and indefinite. It's not clear what an input pattern is and how it is matched with a pattern stored in the instruction region. Furthermore, the specification did not provide any explanation of the elements of this limitation including input pattern, matching, etc. Also, it is not clear what the applicant meant by performing a "reuse", no clear explanation from the specification either. With regards to the last portion of the limitation "outputted to the register and/or the main memory means", this feature appears to be redundant because the third limitation already states that "a register by which the first computing means reads out or writes data to/from the main memory means", wherein the outputted data is outputted to the register and to the memory.

20. Claim 1 recites "*a dependency relations storage section which indicates from which input element in the input pattern each output element in the output pattern derives",* this limitation is vague and indefinite. There is no previously mentioning or defining the input and output element. Thus, these elements lacks of antecedent basis. Furthermore, there is nothing in the claim about "pattern derives". It appears that this

limitation as a whole is omitting an essential element, such omission amounting to a gap between the elements. See MPEP § 2172.01.

21. Claim 1 also recites "*input/output group setting means for setting, based on information stored in the dependency relations storage section, an input/output group which is made up of an output pattern including at least one said output element and an input pattern including at least one said input element",* this limitation is also vague and indefinite. There is no information stored in the dependency relations storage section in the claim, thus there appear to be a missing essential element to show that information is stored in the dependency relations storage. Also, "at least one said output element....and at least one said input element" lack of antecedent basis in the claim.

22. As per claims 2-3, the claims appear to be vague and indefinite. It is not clear what the claim limitation pertains to. For instance, "in a case where a first group of input elements from which a first output element derives is all included in a second group of input elements from which a second output element different from the first output element derives, the input/output group setting means" is vague and unclear, one of ordinary skill in the relevant art would not understand as to what it pertains. Furthermore, there is no clear explanation in the specification.

23. As per claim 5, the claim language is vague and unclear. More specifically, it is unclear of what's meant by several limitation such "in a case where readout from the register and/or memory is carried out...", "(1) when an address of the register and/or the

main memory means from which the readout is carried out has been registered, as an output element....", (2)-(5) is also unclear. Also, some of these limitations 1-5 also lack of antecedent basis. A more precise clarification of the claim language is required. The claim language is indefinite and is interpreted by the examiner as broadly as reasonable possible. It is suggested the applicant's re-write the claims in order to receive a proper and more accurate prosecution.

24. As per claims 6-17, the claim language as currently recited is in coherent and replete with grammatical errors. Examples are shown in claims 1-5 above. The claim language is thus indefinite and is interpreted by one of ordinary skill in the relevant art as broadly as reasonably possible. It is suggested that the applicant's re-write the claims in order to receive a proper and more accurate prosecution since the claims appears to be a translation. The MPEP, in particular, rather than requiring that the claims are insolubly ambiguous, holds that if a claim is amenable to two or more plausible claim constructions, the USPO is justified in requiring the applicant to more precisely define the metes and bounds of the claimed invention by holding the claim unpatenable under 35 USC 112, second paragraph, as indefinite.

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 1-17, 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miki U.S. Patent No. 6,810,474 in view of Huang U.S. Patent No. 4,943,909.

27. As per claim 1, Miki teaches a data processing device which reads out an instruction region from main memory means and writes a result of a computation into the main memory means (see Fig. 1 and col. 4, lines 8-41),

the data processing device comprising:

first computing means for performing a computation based on the instruction region read out from the main memory means (see Fig. 1, and col. 4, lines 35-40);

a register by which the first computing means reads out or writes data to/from the main memory means (Fig. 1, element 118);

input/output generating means for generating an input/output group which is made up of an input pattern and an output pattern at the time of execution of the instruction region by the first computing means (Fig. 3, and col. 8, lines 43-67); and

instruction region storage means for storing the input/output group generated by the input/output generating means (col. 8, line 43 to col. 9, line 8),

at the time of execution of the instruction region, if the input pattern of the instruction region is matched with an input pattern stored in the instruction region storage means, the first computing means performing reuse so that the output pattern, which is stored in the instruction region storage means in association with the input

pattern, is outputted to the register and/or the main memory means (Fig. 3 and col. 8, line 43 to col. 9, line 8; see also col. 9, line 62 to col. 10, line 26), and

Miki shows dependency relations storage (see col. 2, line 8-44) but did not specifically go into the details of input element and output element derives. However, Huang teaches indication from which input element in the input pattern each output element in the output pattern derives; and input/output group setting means for setting, based on information stored in the dependency relations storage section, an input/output group which is made up of an output pattern including at least one said output element and an input pattern including at least one said input element (see Huang, Fig. 3 and col. 5, lines 16-51), for the purpose of realization of any computing function with a regular array of interconnected processing elements.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Huang in invention of Miki, for the purpose of realization of any function within a regular array of interconnected elements thus allowing highly parallel computations which significantly improves performances.

28. As per claim 2, Miki in view of Huang further teaches the data processing device as defined in claim 1, wherein,

in a case where a first group of input elements from which a first output element derives is all included in a second group of input elements from which a second output element different from the first output element derives, the input/output group setting

means sets (i) the second group as the input pattern and (ii) the first group and the second group as the output pattern (see Huang, col. 5, lines 16-67 and see also Miki col. 8, lines 43-67).

29. As per claim 3, Miki in view of Huang further teaches the data processing device as defined in claim 1, wherein,

in a case where there is no shared input element between a first group of input elements from which a first output element derives and a second group of input elements from which a second output element different from the first output element derives, the input/output pattern group setting means sets (i) a first input/output group in which the first group of the input elements is the input pattern and the first output element is the output pattern and (ii) a second input/output group in which the second group of the input elements is the input pattern and the second output element is the output pattern (see Huang, col. 5, lines 16-67 and see also Miki col. 8, lines 43-67).

30. As per claim 4, Huang further teaches the data processing device as defined in claim 1, wherein,

the dependency relations storage section is made up of a 2D-arranged memory in which the output elements are row elements and the input elements are column elements, and each of memory elements of the 2D-arranged memory has information regarding whether or not an output element corresponding to a row element of the memory element is derived from an input element corresponding to a column element of

the memory element (see Huang, Fig. 3 and col. 5, lines 16-67).

31. As per claim 5, Miki in view of Huang further teaches the data processing device as defined in claim 4, wherein,

in a case where readout from the register and/or the main memory means is carried out when the first computing means performs the calculation of the instruction region (see Miki Fig. 1, element 118), the input/output generating means performs:

(1) when an address of the register and/or the main memory means from which the readout is carried out has been registered, as an output element, in the dependency relations storage section, a process to temporarily store a provisional matrix which is made up of a row element, of the dependency relations storage section, which element corresponds to the output element (Huang, Fig. 3 and col. 5, lines 16-67);

(2) when an address of the register and/or the main memory means from which the readout is carried out is registered, as an input element rather than an output element, in the dependency relations storage section, a process to temporarily store a provisional matrix in which a memory element corresponding to a column, of the dependency relations storage section, which column corresponds to the input element is set at 1, and remaining memory elements are set at 0 (see Huang Fig. 6, 8 and col. 8, lines 1-59); and

(3) when an address of the register or the main memory means from which the readout is carried out is registered, in the dependency relations storage section, as neither an output element nor an input element, a process to (i) register, as input

elements, the address and its value in the dependency relations storage section, (ii) temporarily store a provisional matrix in which a memory element corresponding to a column, of the dependency relations storage section, which corresponds to the input element is set at 1, and remaining memory elements are set at 0,in a case where writing is carried out to the register and/or the main memory means, the input/output generating means performs (Huang Fig. 6, 8 and col. 8, lines 1-59 and col. 5, lines 16-67):

(4) when an address of the register and/or the main memory means to which the writing is carried out is registered as an output element, a process to (iii) update an output value corresponding to the registered output element to the written value, (iv) replace a row element, of the dependency relations storage section, which element corresponds to the registered output element, with a logical OR of all provisional matrices temporarily stored at the time, and (v) then initialize the temporarily-stored provisional matrices (Huang, Fig. 12, and col. 10, lines 24-60); and

(5) when an address of the register and/or the main memory means to which the writing is carried out is not registered as an output element, a process to (vi) register the address and its value, as output elements, in the dependency relations storage section, (vii) replace a row element, of the dependency relations storage section, which corresponds to the output element, with a logical OR of all provisional matrices temporarily stored at the time, and (viii) then initialize the temporarily-stored provisional matrices (Huang col. 10, lines 24-60 and col. 8, lines 1-59).

32. As per claim 6, Huang further teaches the data processing device as defined in claim 4, wherein,

the input/output group setting means includes a rows AND comparison section which performs a logic operation AND of the row elements in the 2D-arranged memory (Huang, Fig. 3 and col. 5, lines 16-67), and

in the dependency relations storage section, the input/output group setting means (i) extracts a group of row elements in which a logical AND of an inversion of a first row element and a second row element is all 0, and (ii) among the extracted group of the row elements, excludes, from a candidate as the input/output group, row elements other than a row element which includes the largest number of the input elements (col. 10, lines 24-60 and col. 8, lines 1-59).

33. As per claim 7, Huang further teaches the data processing device as defined in claim 4, wherein,

the input/output group setting means includes a rows AND comparison section which performs a logic operation AND of the row elements in the 2D-arranged memory, and in the dependency relations storage section, the input/output group setting means sets, as the input/output group, a row element whose logical AND with any other row elements is all 0 (col. 10, lines 24-60 and col. 8, lines 1-59; see also col. 5, lines 16-67).

34. As per claim 8, Huang further teaches the data processing device as defined in any claim 1, further comprising at least one second computing means,

in regard of the instruction region processed by the first computing means, the second computing means subjecting the instruction region to a computation based on a predicted input value which is assumed to be inputted hereafter, and registering a result of the computation in the instruction region storage means (col. 5, lines 16-51).

35. As per claim 9, Miki further teaches the data processing device as defined in claim 1, wherein,

the input/output group setting means includes: an output side group storage section which stores information of an input/output group to which each of the output elements belongs; an input side group storage section which stores information of an input/output group to which each of the input elements belongs; a temporal storage section which stores a changed dependency relation between an output element and an input element, when there is a change in the dependency relations storage section while the input/output group is generated; and a group temporal storage section which stores information of a changed input/output group when there is a change in the dependency relations storage section while the input/output group is generated (Fig. 3, and col. 8, lines 43-67 and col. 4, lines 35-40).

36. As per claim 10, Miki further teaches the data processing device as defined in claim 9, wherein,

the input/output group setting means further includes a group management section that stores information of the input/output group which has already been

allocated to the output element and/or the input element, while the input/output group is generated (Fig. 3, and col. 8, lines 43-67 and col. 8, line 43 to col. 9, line 8),

37. As per claim 11, Huang further teaches the data processing device as defined in claim 9, wherein,

the dependency relations storage section is made up of a 2D-arranged memory in which the output elements are row elements and the input elements are column elements, and each of memory elements of the 2D-arranged memory has information regarding whether or not an output element corresponding to a row element of the memory element is derived from an input element corresponding to a column element of the memory element (see Huang, Fig. 3 and col. 5, lines 16-67).

38. As per claim 12, Huang further teaches the data processing device as defined in claim 11, wherein,

the temporal storage section stores a logical OR of memory elements of a plurality of rows in the dependency relations storage section, and the group temporal storage section stores (i) a logical OR of memory elements of a plurality of rows in the output side group storage section and/or (ii) a logical OR of memory elements corresponding to a plurality of input elements in the input side group storage section (col. 10, lines 24-60 and col. 8, lines 1-59; see also col. 5, lines 16-67).

39. As per claim 13, Miki further teaches the data processing device as defined in claim 9, wherein,

the input/output group setting means further includes a conditional branch storage section which stores, when a conditional branch instruction is detected while the input/output group is generated, information regarding an input element on which the conditional branch instruction depends (see col. 4, lines 8-41).

40. As per claim 14, Miki in view of Huang further teaches the data processing device as defined in claim 12, wherein,

in a case where readout from the register and/or the main memory means is carried out while the first computing means performs a calculation of the input region see Miki Fig. 1, element 118), the input/output generating means performs:

(1) when an address of the register and/or the main memory means from which the readout is carried out has been registered, as an output element, in the dependency relations storage section, a process to temporarily store, in the temporal storage section, a logical OR of (i) a row element, of the dependency relations storage section, which corresponds to the output element and (ii) the elements in the temporal storage section, and store, in the group temporal storage section, a logical OR of (iii) a row element, of the output side group storage section, which corresponds to the output element and (iv) the elements in the group temporal storage section (Huang, Fig. 3 and col. 5, lines 16-67);

(2) when an address of the register and/or the main memory means from which the readout is carried out is registered, as an input element rather than an output element, in the dependency relations storage section, a process to store, in the temporal storage section, information in which a memory element corresponding to a column, of the dependency relations storage section, which corresponds to the input element is set at 1 and remaining memory elements are set at 0, and store, in the group temporal storage section, a logical OR of (v) elements, in the input side group storage section, which correspond to the input element and (vi) the elements in the group temporal storage section (see Huang Fig. 6, 8 and col. 8, lines 1-59); and

(3) when an address of the register and/or the main memory means from which the readout is carried out is not registered in the dependency relations storage section as either an output element or an input element, a process to register, as input elements, the address and its value in the dependency relations storage section, and temporarily store a provisional matrix in which a memory element corresponding to a column, of the dependency relations storage section, which corresponds to the input element is set at 1 while remaining memory elements are set at 0 (Huang Fig. 6, 8 and col. 8, lines 1-59 and col. 5, lines 16-67);

in a case where writing is carried out to the register and/or the main memory means, the input/output generating means performs:

(4) when an address of the register and/or the main memory means to which the writing is carried out is registered as an output element, a process to update an output value corresponding to the registered output element to the written value, replace a row

element, of the dependency relations storage section, which corresponds to the registered output element, with the information temporarily stored in the temporal storage section at the time, and update (viii) the information in the output side group storage section, which information corresponds to the output element, and (ix) the information in the input side group storage section, which information corresponds to the input elements on which the output element depends, based on the information stored in the group temporal storage section (Huang, Fig. 12, and col. 10, lines 24-60); and

(5) when an address of the register and/or the main memory means to which the writing is carried out is not registered as an output element, a process to register the address and its value, as output elements, in the dependency relations storage section, replace a row element, of the dependency relations storage section, which corresponds to the output element, with the information temporarily stored in the temporal storage section at the time, and update (x) the information, in the output side group storage section, which information corresponds to the output element, and (xi) the information, in the input side group storage section, which information corresponds to the input elements on which the output element depends, based on the information stored in the group temporal storage section (Huang col. 10, lines 24-60 and col. 8, lines 1-59).

41. As per claim 15, Miki further teaches the data processing device as defined in claim 1, wherein, the instruction region storage means includes input pattern storage means which stores the input patterns as a tree structure in which items to be subjected

to equal comparison are regarded as nodes (Fig. 3, and col. 8, lines 43-67).

42. As per claim 16, Miki further teaches the data processing device as defined in claim 15, wherein,

the input pattern storage means realizes the tree structure in such a manner that a value of an item in the input pattern, which item is subjected to equal comparison, is stored in association with an item to be subjected to comparison next (see col. 8, lines 15-67).

43. As per claim 17, Huang further teaches the data processing device as defined in claim 16, wherein, the input pattern storage means includes associative search means and additional storage means, the associative search means includes one or more search target line which includes: a value storage area where a value of an item to be subjected to equal comparison is stored; and a key storage area where a key for identifying each item is stored, and the additional storage means has a search item designation area in which an item to be subjected to associative search next is stored in accordance with a corresponding line corresponding to said one or more search target line (col. 10, lines 24-60 and col. 8, lines 1-59).

44. As per claim 30, it is rejected for the same reasons set forth above in claim 1.

45. As per claim 31, Miki further teaches a computer-readable storage medium, storing the data processing program defined in claim 30 (see Fig. 1, element 108).

Conclusion

46. Any inquiry concerning this communication or earlier communications from the examiner should be directed to IDRISS N. ALROBAYE whose telephone number is (571)270-1023. The examiner can normally be reached on Mon-Fri from 8:00 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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